AN-1732 LP38501TS-ADJ Evaluation Board

1 Introduction

The LP38501TS-ADJ is a 3A low-dropout (LDO) linear regulator with adjustable output voltage that is set by external resistors.

2 Basic Application Circuit

The basic application circuit which is built up on the evaluation board is shown in Figure 1.

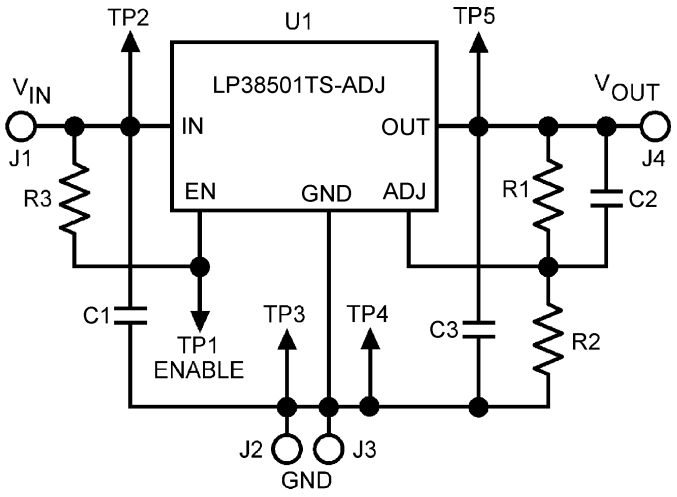

Figure 1. Schematic for Basic Application Circuit

3 Changing the Output Voltage

The resistors R1 and R2 set the output voltage. Equation 1 determines the output voltage:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (1)$$

The board has installed values of 19.1 kΩ for R1 and 6.04 kΩ for R2, which sets the output to 2.50 V.

$$V_{OUT} = 0.60\ V \times (1 + (19.1k\Omega / 6.04\ k\Omega)) \quad (2)$$

$$V_{OUT} = (0.60\ V \times 4.162) = 2.497\ V \quad (3)$$

R1 can be adjusted to change the nominal output voltage to other values. The minimum output voltage that can be set is the ADJ pin voltage, which is approximately 0.6 V. This is obtained by installing a jumper or low value resistor (less than 10 Ω) at R1. The maximum usable output voltage is limited by the maximum input voltage which is 5.5 V. Since rated dropout voltage at full current is 0.375 V, this means the maximum usable output voltage for full current operation is about 5.1 V.

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4 Feedforward Capacitor C2

The PCB layout includes a location for C2, which is a feedforward capacitor connected across R1. If the data sheet guidelines are followed, and R2 does not exceed 10 kΩ, C2 is not required and has no effect on performance. The internal compensation is such that an internal zero provides more than adequate phase margin so external compensation is never needed.

However, if the value of R2 is increased above 10 kΩ, the effect of the internal zero gradually diminishes and the phase margin is reduced. At an R2 value of approximately 50 kΩ, the phase margin will be low enough that instability may occur. In such cases, some of the lost phase margin can be regained by placing a capacitor at C2. Although it is sometimes possible to regain adequate phase margin this way, it is recommended that the data sheet guidelines be followed and R2 not exceed 10 kΩ (so C2 is never required).

5 Power Dissipation

The power dissipated within the regulator IC is given by:

$$P_D = I_L (V_{IN} - V_{OUT}) \quad (4)$$

Where:

$\mathbf{P_D}$ is the power dissipated in the IC regulator U1

$\mathbf{I_L}$ is the load current

$\mathbf{V_{IN}}$ is the value of V_{IN} measured at TP2 (not at J1)

$\mathbf{V_{OUT}}$ is the value of V_{OUT} measured at TP5 (not at J4)

The thermal resistance of U1 from junction to ambient can be assumed to be approximately 30°C/W for this assembly. That means that the junction temperature will rise about 30°C above ambient for each Watt of power dissipated within the IC.

Since the parametric specifications of the IC are for a maximum junction temperature of 125°C, this limits maximum usable power dissipation to approximately 4W. If power dissipation exceeds this (and the junction temperature approaches 150°C), the part may go into thermal shutdown.

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6 PCB Component Layout

The components listed in the basic application circuit can be identified using the silkscreen on the top layer of the PCB (see Figure 2).

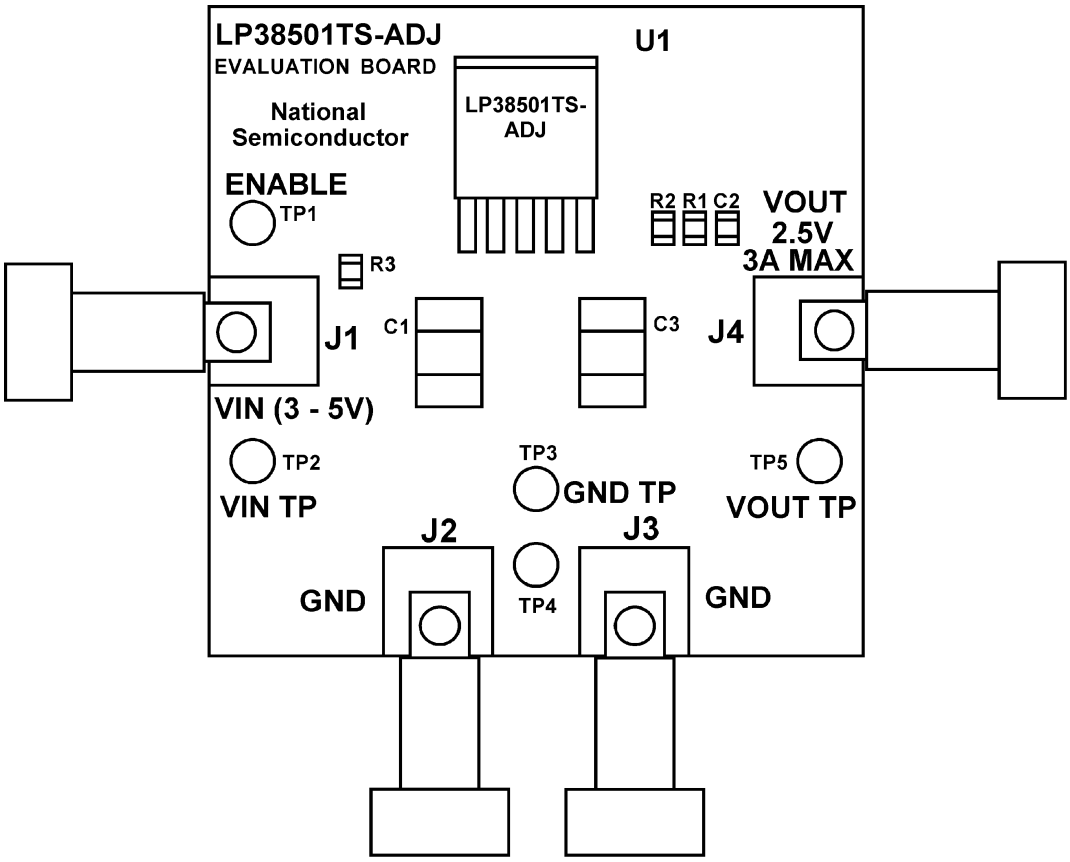

Figure 2. PCB Assembly (Top View)

7 Bill of Materials (BOM)

The initial evaluation boards were built up for a 2.5 V regulated output. The components used in the PCB assembly are listed in Table 1.

Table 1. Bill of Materials (BOM)

Qty	Designator	Component	Manufacturer
1	PCB	PC board	NSC# 980013247-100A
1	R1	Resistor, 19.1k, 1%	VISHAY CRCW08051912F
1	R2	Resistor 6.04k, 1%	VISHAY CRCW08056041F
1	R3	Resistor, 51.1k, 1%	VISHAY CRCW08055112F
1	J1	Red Banana Jack	Digi-Key J-151-ND
2	J2, J3	Black Banana Jack	Digi-Key J-152-ND
1	J4	Blue Banana Jack	Digi-Key J-155-ND
2	C1, C3	Cap, CER, 22 µF	Digi-Key PCC2228CT-ND
5	TP1 - TP5	Test Points	Newark 160-2043-02-01-00
1	U1	IC, LP38501	TI LP38501
	C2	**** NOT INSTALLED FOR THIS ASSEMBLY	

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